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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A programmable gain voltage buffer comprising:
a gain stage;
a programmable resistance coupled in series and in communication with the gain stage,
the programmable resistance including a plurality of switches in parallel with a reference
resistive element; and
an output node coupled between the gain stage and the programmable resistance,
wherein the plurality of switches are operable to change a gain at the output node.
2. (Canceled)
3. (Previously Presented) The voltage buffer of claim 1, wherein the gain at the output
node has a first gain value when a switch of the plurality of switches is activated and a second
gain value when the switch is deactivated.
4. (Currently Amended) A programmable gain voltage buffer comprising:
a gain stage;
a programmable resistance coupled in series and in communication with the gain stage,
the programmable resistance including a plurality of switches in parallel with a reference
resistive element; and

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an output node coupled between the gain stage and the programmable resistance,
wherein the plurality of switches are operable to change a gain at the output node, at least one switch being used as a variable resistance to adjust an effective resistance value at the output node, and the gain is proportional to an equivalent resistance at the output node.

5. (Previously Presented) The voltage buffer of claim 1, wherein the plurality of switches are operable to change the gain in response to being activated and deactivated.

6. (Currently Amended) The voltage buffer of claim 1, wherein a switch of the plurality of switches provides a first resistance value in parallel with the reference resistive element when activated and is effectively removed when deactivated.

7. (Original) The voltage buffer of claim 6, wherein the first resistance value comprises a source-drain resistance of the switch.

8. (Previously Presented) The voltage buffer of claim 6, wherein the first resistance value of the switch corresponds to a programmable gain step for a circuit comprising the programmable resistance.

9. (Currently Amended) The voltage buffer of claim 1, wherein the voltage buffer comprises a differential voltage buffer including two branches, each branch including a gain stage, and

a programmable resistance coupled in series and in communication with the gain stage, the programmable resistance including a plurality of switches in parallel with a reference resistive element.

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10. (Previously Presented) The voltage buffer of claim 9, wherein at least one switch from each of the two branches are together operative to be activated and deactivated substantially simultaneously.

11. (Canceled)

12. (Currently Amended) The voltage buffer of claim 1, further comprising a [second] circuit operative to control an accuracy of the gain.

13. (Currently Amended) A programmable gain voltage buffer comprising:

a gain stage;

a programmable resistance in communication with the gain stage, the programmable resistance including a switch in parallel with a resistive element; and

a [second] circuit operative to control an accuracy of the gain, the [second] circuit comprising:

a reference resistive element;

a tunable resistive element in parallel with the reference resistive element, the tunable resistive element operative to track a resistance of the reference resistive element and having a gate with a bias voltage; and

an output line coupled to the gate of the tunable resistive element and a gate of the switch.

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14. (Previously Presented) A method comprising:
applying an input signal to a voltage buffer;
activating one or more selected switches in a plurality of switches in parallel with a predominant reference resistive element in the voltage buffer; and
changing a gain of the buffer by at least a programmable gain step;
wherein said changing the gain is realized at an output node coupled between a gain stage and a programmable resistance of the voltage buffer, the gain stage and the programmable resistance being configured in series.

15. (Currently Amended) A method comprising:
applying an input signal to a voltage buffer;
activating one or more selected switches in parallel with a predominant reference resistive element in the voltage buffer;
changing a gain of the buffer by at least a programmable gain step by changing an equivalent resistance at an output point in the voltage buffer using the one or more selected switches as a variable resistance to adjust an effective resistance value at the output point; and
providing an output signal from the output point coupled between a gain stage and a programmable resistance of the voltage buffer, wherein the gain stage and the programmable resistance are configured in series.

16. (Canceled)

17. (Original) The method of claim 14, wherein said applying the input signal comprises receiving a signal from a first circuit.

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18. (Original) The method of claim 17, further comprising:

providing an output signal to a second circuit.

19. (Original) The method of claim 18, wherein the first circuit comprises a reference voltage circuit.

20. (Original) The method of claim 19, wherein the second circuit comprises a load circuit.

21. (Currently Amended) A device comprising:

a first circuit operative to provide a voltage signal;

a second circuit;

a voltage buffer coupled between the first and second circuits and operative to provide a programmable gain to the voltage signal, the voltage buffer comprising:

a gain stage;

a programmable resistance coupled in series and in communication with the gain stage, the programmable resistance including a plurality of switches in parallel with a reference resistive element; and

an output node coupled between the gain stage and the programmable resistance, wherein the plurality of switches are operable to change a gain at the output node.

22. (Canceled)

23. (Previously Presented) The device of claim 21, wherein the gain at the output node has a first gain value when a switch of the plurality of switches is activated and a second gain value when the switch is deactivated.

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24. (Currently Amended) A device comprising:

a first circuit operative to provide a voltage signal;

a second circuit;

a voltage buffer coupled between the first and second circuits and operative to provide a programmable gain to the voltage signal, the voltage buffer comprising:

a gain stage;

a programmable resistance coupled in series and in communication with the gain stage, the programmable resistance including a plurality of switches in parallel with a reference resistive element; and

an output node coupled between the gain stage and the programmable resistance,

wherein the plurality of switches are operable to change a gain at the output node, at least one switch being used as a variable resistance to adjust an effective resistance value at the output node, and the gain is proportional to an equivalent resistance at the output node.

25. (Previously Presented) The device of claim 21, wherein the plurality of switches are operable to change the gain in response to being activated and deactivated.

26. (Currently Amended) The device of claim 21, wherein the programmable resistance comprises a third circuit, and

wherein [the] at least one switch provides a first resistance value in parallel with the reference resistive element when activated and is effectively removed from the third circuit when deactivated.

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27. (Original) The device of claim 26, wherein the first resistance value comprises a source-drain resistance of the switch.

28. (Previously Presented) The device of claim 26, wherein the first resistance value of the switch corresponds to a programmable gain step for the third circuit.

29. (Currently Amended) The device of claim 21, wherein the voltage buffer comprises a differential voltage buffer including two branches, each branch including
a gain stage, and
a programmable resistance coupled in series and in communication with the gain stage,
the programmable resistance including a plurality of switches in parallel with a reference
resistive element

30. (Previously Presented) The device of claim 29, wherein at least one switch from each of the two branches are together operative to be activated and deactivated substantially simultaneously.

31. (Canceled)

32. (Previously Presented) The device of claim 21, further comprising a third circuit operative to control an accuracy of the gain.

33. (Previously Presented) A device comprising:
a first circuit operative to provide a voltage signal;
a second circuit;
a voltage buffer coupled between the first and second circuits and operative to provide a programmable gain to the voltage signal, the voltage buffer comprising:

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a gain stage;

a programmable resistance in communication with the gain stage, the programmable resistance including a switch in parallel with a resistive element; and

a third circuit operative to control an accuracy of the gain, the third circuit comprising:

a reference resistive element;

a tunable resistive element in parallel with the reference resistive element, the tunable resistive element operative to track a resistance of the reference resistive element and having a gate with a bias voltage; and

an output line coupled to the gate of the tunable resistive element and a gate of the switch.

34. (Currently Amended) A programmable gain voltage buffer comprising:

a gain stage;

means for providing a programmable resistance coupled in series and in communication with the gain stage, the programmable resistance including plural switching means in parallel with reference resistive means; and

an output node coupled between the gain stage and the programmable resistance, wherein the switching means includes means for changing a gain at the output node.

35. (Canceled)

36. (Previously Presented) The voltage buffer of claim 34, wherein the gain at the output node has a first gain value when the switching means is activated and a second gain value when the switching means is deactivated.

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37. (Currently Amended) A programmable gain voltage buffer comprising:

a gain stage;

means for providing a programmable resistance coupled in series and in communication with the gain stage, the programmable resistance including plural switching means in parallel with reference resistive means; and

an output node coupled between the gain stage and the programmable resistance,

wherein at least one switching means includes means for changing a gain at the output node, the at least one switching means being used as a variable resistance to adjust an effective resistance value at the output node, and the gain is proportional to an equivalent resistance at the output node.

38. (Previously Presented) The voltage buffer of claim 34, wherein the switching means is operable to change the gain in response to being activated and deactivated.

39. (Currently Amended) The voltage buffer of claim 34, wherein the switching means provides a first resistance value in parallel with the reference resistive means when activated and is effectively removed when deactivated.

40. (Original) The voltage buffer of claim 39, wherein the first resistance value comprises a source-drain resistance of a switch.

41. (Previously Presented) The voltage buffer of claim 39, wherein the first resistance value of the switching means corresponds to a programmable gain step for a circuit comprising the programmable resistance.

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42. (Currently Amended) The voltage buffer of claim 34, wherein the voltage buffer comprises a differential voltage buffer including two branches, each branch including a gain stage, and means for providing a programmable resistance coupled in series and in communication with the gain stage, the programmable resistance including plural switching means in parallel with reference resistive means

43. (Previously Presented) The voltage buffer of claim 42, wherein at least a portion of the switching means in the two branches are operative to be activated and deactivated substantially simultaneously.

44. (Canceled)

45. (Currently Amended) The voltage buffer of claim 34, further comprising a [second] circuit including means for controlling an accuracy of the gain.

46. (Currently Amended) A programmable gain voltage buffer comprising:
a gain stage;
means for providing a programmable resistance in communication with the gain stage, the programmable resistance including switching means in parallel with resistive means; and
a [second] circuit including means for controlling an accuracy of the gain, the second circuit comprising:

means for providing a reference resistance;

means for providing a tunable resistance in parallel with the means for providing the reference resistance, the means for providing the tunable resistance including means

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for tracking a resistance of the reference resistive means and having a gate with a bias
voltage; and

an output line coupled to said gate and a gate of the switching means.